REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on March 20, 2003, and the references cited therewith. No claims are amended or cancelled. Claims 19-43 remain pending in this application.

The amendment filed December 2, 2002 was objected to under 35 USC § 132. The objection stated that the amendment introduced new matter into the disclosure.

Applicant respectfully traverses this objection and respectfully submits that no new matter was added. Applicant respectfully submits that use of embodiments of Applicant's invention in a memory device are discussed and supported on page 1, lines 8-16. Applicant further submits that one of ordinary skill in the art will recognize that a memory device includes DRAM's which in turn include an array of memory cells.

§112 Rejection of the Claims

Claims 19-43 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The rejections state that, "There is no original disclosure relating to forming an integrated circuit. There is no original disclosure relating to dynamic random access memory (DRAM) or to an array of memory cells."

Applicant respectfully traverses the rejection and submits that use of embodiments of Applicant's invention in a memory device are discussed and supported on page 1, lines 8-16. Applicant further submits that one of ordinary skill in the art will recognize that a memory device includes DRAM's which in turn include an array of memory cells.

The rejection further states that, "In order to be a voltage regulator a device has to sense a voltage level at a point where the voltage is to be regulated and control the voltage at that point."

Applicant respectfully submits that the level of detail needed for one of ordinary skill in the art to make and use the invention is disclosed in the present specification. For example, in the absence of additional details regarding a sensing operation, Applicant respectfully submits that upon reading the specification, one of ordinary skill in the art will understand how to implement a sensing operation in embodiments of the present invention.

Reconsideration and withdrawal of the 35 USC § 112, first paragraph rejections is respectfully requested.

Claims 19-43 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The rejection states that, "It is still not clear how the voltage regulator is coupled to the substrate." Applicant respectfully submits that "coupling" is definite under 35 USC § 112, second paragraph. Pursuant to MPEP § 2173.04, Applicant notes that "breadth of a claim is not to be equated with indefiniteness." Examples of coupling elements of a voltage regulator include, but are not limited to, utilizing MOS fabrication techniques to form elements such as transistors or diodes as described in the specification. In further example, a source/drain region of a MOS transistor formed by ion implantation is coupled to a substrate.

Reconsideration and withdrawal of the 35 USC § 112, second paragraph rejections is respectfully requested.

§103 Rejection of the Claims

Claims 19-43 were rejected under 35 USC § 103(a) as being unpatentable over McLaury in view Bynum et al, Yim and Sawamura.

The rejection states that, "McLaury shows apparatus for regulating substrate bias." McLaury appears to show a diode series 10. The reference also appears to show a diode load element 110. Embodiments of McLaury also appear to show a sense element as part of the integrated circuit. However, Applicant is unable to find at least one **bypass transistor** to at least one diode in a series of diodes for electrically bypassing at least one diode. In contrast,

Applicant's independent claims all include at least one bypass transistor to at least one diode in a series of diodes for electrically bypassing at least one diode.

The rejection states that, "Bynum et al shows the concept of controlling the bias applied to a substrate by shunting a diode in a line that applies a voltage to a substrate." Bynum appear to show an integrated circuit designed to bias an epitaxial well. Embodiments of Bynum appear to include a single diode 42. Bynum also appears to show a shunt path in embodiments using the diode. However, Applicant is unable to find at least one **bypass transistor** to at least one diode in a **series of diodes** for electrically bypassing at least one diode. Applicant respectfully submits that a shunt is not equivalent to a bypass transistor. In contrast, Applicant's independent claims all include at least one bypass transistor to at least one diode in a series of diodes for electrically bypassing at least one diode.

The rejection states that, "Yim et al shows that plural diodes may be used in a line to tailor the applied voltage." Yim appears to show a voltage drop stage 10 that includes a plurality of MOSFET's whose gates are connected with their drains. However, Yim does not show at least one **bypass transistor** to at least one diode in a series of diodes for electrically bypassing at least one diode. In contrast, Applicant's independent claims all include at least one bypass transistor to at least one diode in a series of diodes for electrically bypassing at least one diode.

Applicant respectfully submits that Sawamura does not cure the deficiencies of the references discussed above.

The pending Office Action asserts that arguments presented in the previous response were argued "as if each reference is applied solely in a 35 U.S.C. 102 rejection." Applicant respectfully appreciates the nature of an obviousness rejection under 35 USC § 103, and submits that present arguments and previous arguments address the rejection as required under 35 USC § 103. Previous argument was intended to show consistent deficiencies in each reference such that when combined, there remained elements of Applicant's claims that were not shown in the combination of references. For example, as shown in emphasis in the arguments presented above, Applicant is unable to find at least one **bypass transistor** to at least one diode in a series of diodes for electrically bypassing at least one diode in any of the references taken alone. Therefore the combination of references also lacks this element. No combination of the references shows, teaches, or suggests bypassing a portion of a series.

Because the cited references, either alone or in combination, do not show every element of Applicant's independent claims, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claims 19, 22, 27, 30, 33, 37, and 41. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6944 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 5/20/03

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop RCE, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 20th day of May, 2003

Amy Moriarty
Name

Signature